

KAF- 6302LE

3072 (H) x 2034 (V) Pixel

**Enhanced Response
Full-Frame CCD Image Sensor
With Anti-Blooming Protection**

Performance Specification

Eastman Kodak Company

Image Sensor Solutions

Rochester, New York 14650-2010

Revision 1

September 18, 2002



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1. DESCRIPTION

1.1 FEATURES

- **6M Pixel Area CCD**
- **3072H x 2034V (9 μm) Pixels**
- **Transparent Gate True Two Phase Technology**
(Enhanced Spectral Response)
- **27.65 mm H x 18.48 mm V Photosensitive Area**
- **2-Phase Register Clocking**
- **70% Fill Factor**
- **Antiblooming Protection**
- **Low Dark Current (<10pA/cm² @ 25°C)**

1.2 ARCHITECTURE

The KAF-6302LE is a high performance monochrome area CCD (charge-coupled device) image sensor with 3072H x 2034 V photo active pixels designed for a wide range of image sensing applications in the 0.3 nm to 1.0 nm wavelength band. Typical applications include military, scientific, and industrial imaging. A 74dB dynamic range is possible operating at room temperature.

The sensor is built with a true two-phase CCD technology. This technology simplifies the support circuits that drive the sensor and reduces the dark current without compromising charge capacity. The transparent gate results in spectral response increased ten times at 400 nm, compared to a front side illuminated standard poly silicon gate technology. The sensitivity is increased 50% over the rest of the visible wavelengths.

Total chip size is 29.0 mm x 19.1 mm and is housed in a 26-pin, 0.88” wide DIL ceramic package with 0.1” pin spacing.

The sensor consists of 3088 parallel (vertical) CCD shift registers each 2056 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The elements of these registers are arranged into a 3072 x 2034 photosensitive array surrounded by a light shielded dark reference of 16 columns and 20 rows. The parallel (vertical) CCD registers transfer the image one line at a time into a single 3100 element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a two-stage source follower that converts the photo generated charge to a voltage for each pixel.

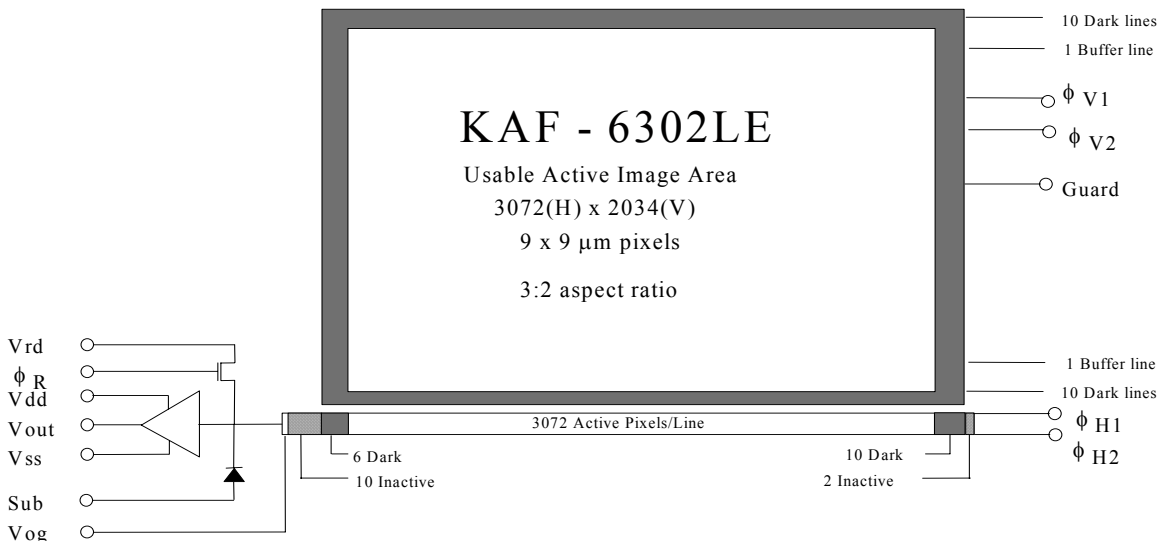


Figure 1 - Functional Block Diagram



1.3 FUNCTIONAL DESCRIPTION

1.3.1 Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon-induced electrons are collected locally by the formation of potential wells at each photo gate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will spill into the lateral overflow drain (LOD) and drain off chip, thus isolating adjacent pixels from the excess signal. This is termed anti-blooming protection. During the integration period, the $\Phi V1$ and $\Phi V2$ register clocks are held at a constant (low) level. See Figure 5. - Timing Diagrams.

The anti blooming capability is provided by a lateral overflow drain structure. This type of anti blooming design consumes thirty percent of the pixel area and reduces the saturation signal and quantum efficiency proportionately. However, it maintains the broad spectral response from 400 to 1000 nm and good linear response up to saturation.

1.3.2 Charge Transport

Referring again to Figure 5 - Timing Diagrams, the integrated charge from each photo gate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCDs to the horizontal CCD register using the $\Phi V1$ and $\Phi V2$ register clocks. The horizontal CCD is presented a new line on the falling edge of $\Phi V2$ while $\Phi H1$ is held high. The horizontal CCDs then transport each line, pixel by pixel, to the output structure by alternately clocking the $\Phi H1$ and $\Phi H2$ pins in a complementary fashion. On each falling edge of $\Phi H2$ a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier

1.3.3 Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on FD. Once the signal has been sampled by the system electronics, the reset gate (ΦR) is clocked to remove the signal and FD is reset to the potential applied by V_{rd} . More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the V_{out} pin of the device - see Figure 4

1.3.4 Dark Reference Pixels

Surrounding the peripheral of the device is a border of light shielded pixels. This includes 6 leading and 10 trailing pixels on every line excluding dummy pixels. There are also 10 full dark lines at the start of every frame and 10 full dark lines at the end of each frame. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel, or the outer bounds of the chip (including the first two lines out), can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

1.3.5 Buffer Rows

The rows adjacent to the dark reference have photo response that is somewhat lower than that of the rest of the photo active rows. For this reason they are not included in the count of photo active rows. They may be useful depending on the application.

1.3.6 Dummy Pixels

Within the horizontal shift register are 10 leading and 2 trailing additional shift phases, which are not associated with a column of pixels from the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions.



1.4 PIN DESCRIPTION

Pin	Symbol	Description	Pin	Symbol	Description
1,13,14,15, 26	Vsub	Substrate (Ground)	10	ϕ_{H1}	Horizontal CCD Clock - Phase 1
2	Vout	Video Output	11	ϕ_{H2}	Horizontal CCD Clock - Phase 2
3	Vdd	Amplifier Supply	16, 17, 22,23	ϕ_{V1}	Vertical CCD Clock - Phase 1
4	Vrd	Reset Drain	18, 19, 20,21	ϕ_{V2}	Vertical CCD Clock - Phase 2
5	ϕ_R	Reset Clock	24	Vguard	Guard Ring
6	Vss	Amplifier Supply Return	25	Vog	Output Gate
7, 8, 9, 12	N/C	No connection (open pin)			

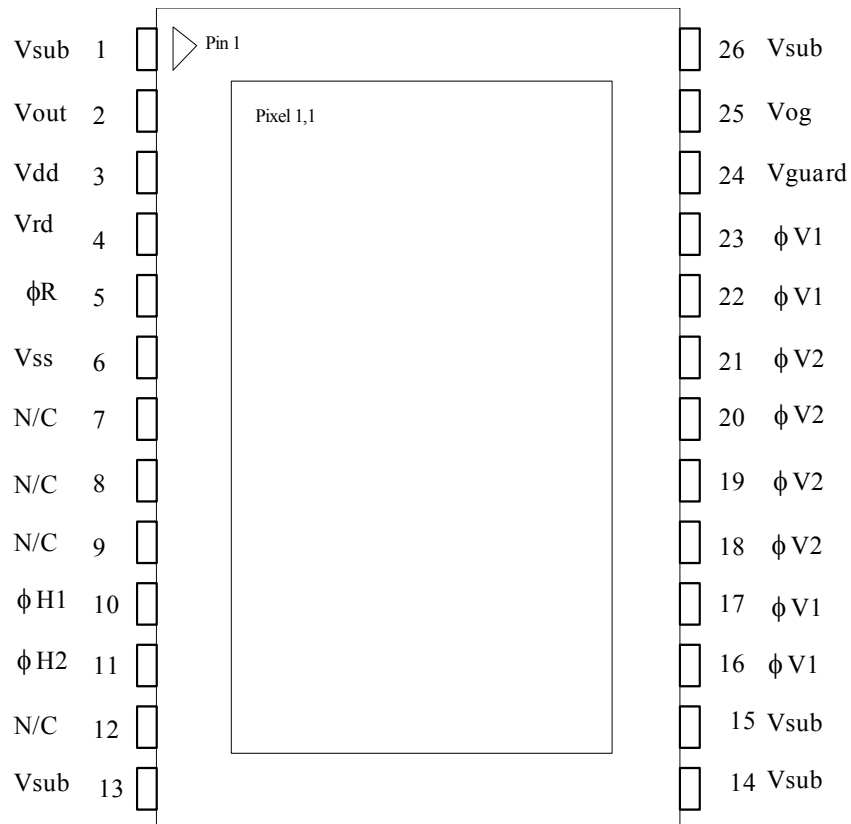


Figure 2 - Pin

Designations



2. IMAGING PERFORMANCE SPECIFICATIONS

2.1 ELECTRO-OPTICAL CHARACTERISTICS

All values measured at 25°C, and nominal operating conditions. These parameters exclude defective pixels.

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Saturation Signal Vertical CCD capacity Horizontal CCD capacity Output Node capacity	Nsat	45000 170000 150000	55000 200000 160000	65000 240000 170000	electrons / pixel	1
Red Quantum Efficiency ($\lambda=650\text{nm}$)	Rr		42		%	
Green Quantum Efficiency ($\lambda=550\text{nm}$)	Rg		35		%	
Blue Quantum Efficiency ($\lambda=450\text{nm}$)	Rb		20		%	
Blue Quantum Efficiency ($\lambda=400\text{nm}$)	Rb 400		16			
Photoresponse Non-Linearity	PRNL		1	2	%	2
Photoresponse Non-Uniformity	PRNU		1	3	%	3
Dark Signal	Jdark		15 2.1	35 7	electrons / pixel / sec pA/cm ²	4
Dark Signal Doubling Temperature		5	6.3	7.5	°C	
Dark Signal Non-Uniformity	DSNU		15	35	electrons / pixel / sec	5
Dynamic Range	DR	67	68		dB	6
Charge Transfer Efficiency	CTE	0.99997	0.99999			
Output Amplifier DC Offset	Vodc		Vrd+1.0		V	7
Output Amplifier Bandwidth	f _{-3dB}		45		Mhz	8
Output Amplifier Sensitivity	Vout/Ne~	9	10	11	uV/e~	
Output Amplifier output Impedance	Zout	175	200	250	Ohms	
Noise Floor	ne~		15	20	electrons	9
Antiblooming Protection	Vab	128			Saturation exposure	10

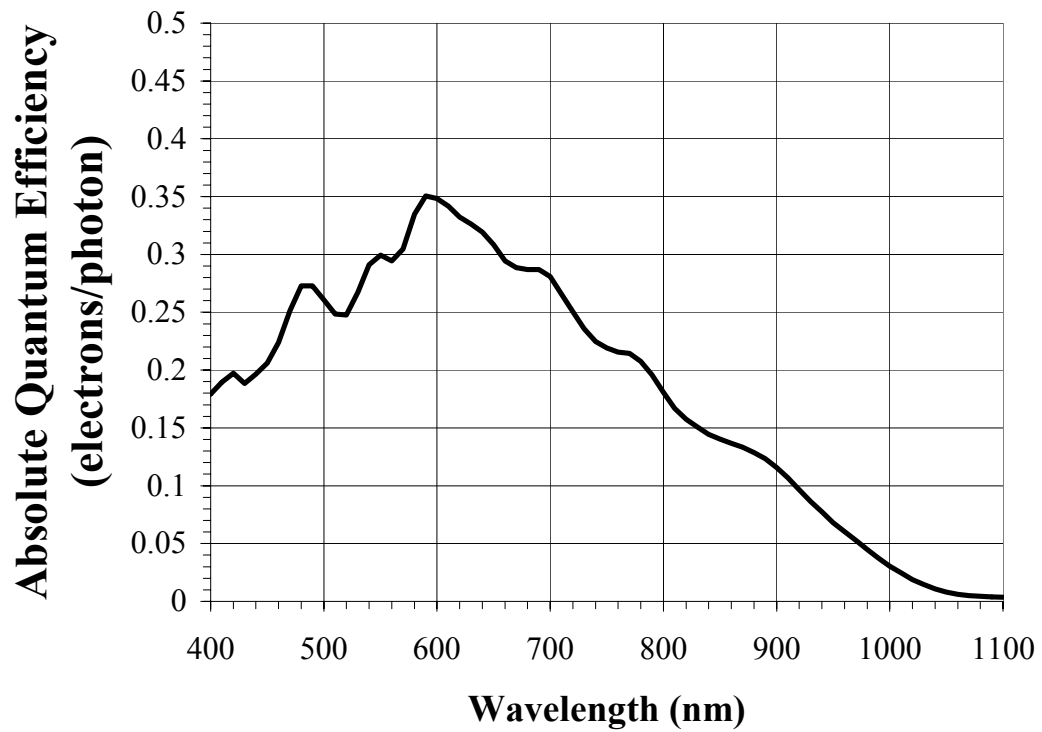
Notes:

- For pixel binning applications, electron capacity up to 320000 can be achieved with modified CCD inputs. Each sensor may have to be optimized individually for these applications. Some performance parameters may be compromised to achieve the largest signals.
- Worst case deviation from straight line fit, between 1% and 90% of Vsat.
- One Sigma deviation of a 128x128 sample when CCD illuminated uniformly.
- Average of all pixels with no illumination at 25°C.
- Average dark signal of any of 12 x 8 blocks within the sensor. (each block is 128 x 128 pixels)
- $20\log (Nsat / ne\sim)$ at nominal operating frequency and 25°C.
- Video level offset with respect to ground
- Last output amplifier stage only. Assumes 10pF off-chip load..
- Output noise of the amplifier at nominal operating frequency, and tint = 0, excluding dark current shot noise. Bandwidth is five times the pixel frequency. Lower noise floor can be achieved at lower pixel frequencies and reduced bandwidth. The noise floor is calculated to be 5 electrons at a pixel frequency of 200 kHz.
- Number of times above the Vsat illumination level required to cause 50% distortion in a test pattern consisting of a bright circular region approximately 1/10 the size of the image sensor. In most systems a 128x optical overload will cause flare from reflections that mask the performance of the image sensor.



2.2 QUANTUM EFFICIENCY

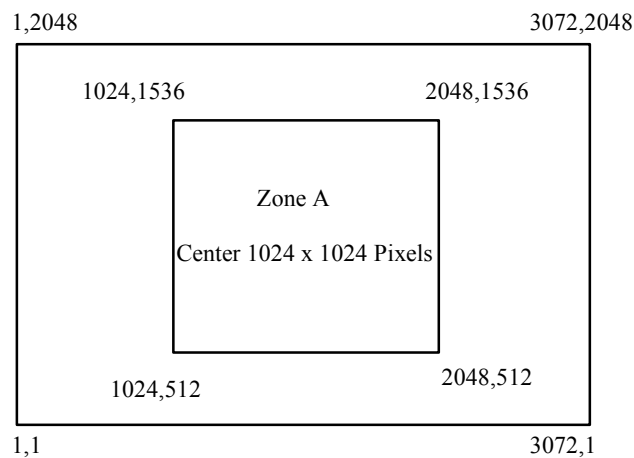
KAF-6302LE



2.3 COSMETIC SPECIFICATION

Defect tests performed at T=25°C

Class	Point Defects		Cluster Defects		Maximum Cluster Size	Column Defects	
	Total	Zone A	Total	Zone A		Total	Zone A
C1	≤22	≤9	0	0	2	0	0
C2	≤45	≤22	≤18	≤9	5	≤5	0
C3	≤90	≤45	≤36	≤18	5	≤9	≤4



Point Defect	Dark: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation, OR Bright: A Pixel with dark current > 3,000 e/pixel/sec at 25C.
Cluster Defect	A grouping of not more than 5 adjacent point defects
Column Defect	A grouping of >5 contiguous point defects along a single column, OR A column containing a pixel with dark current > 7,000e/pixel/sec, OR A column that does not meet the CTE specification for all exposures less than the specified Max sat. signal level and greater than 2 Ke, OR A pixel which loses more than 250 e under 2Ke illumination.
Neighboring pixels	The surrounding 128 x 128 pixels or ±64 columns/rows.
Defect Separation	Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).
Defect Region Exclusion	Defect region excludes the outer two (2) rows and columns at each side/end of the sensor.



3 OPERATION

3.1 ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Min.	Max.	Units	Notes
Diode Pin Voltages	Vdiode	0	20	V	1,2
Gate Pin Voltages - Type 1	Vgate1	-16	16	V	1,3
Gate Pin Voltages - Type 2	Vgate2	0	16	V	1,4
Inter-Gate Voltages	Vg-g		16	V	5
Output Bias Current	Iout		-10	mA	6
Output Load Capacitance	Cload		15	pF	6

Notes:

1. Referenced to pin Vsub.
2. Includes pins: Vrd, Vdd, Vss, Vout, Vguard.
3. Includes pins: $\phi V1$, $\phi V2$, $\phi H1$, $\phi H2$.
4. Includes pins: ϕR , Vog.
5. Voltage difference between overlapping gates. Includes: $\phi V1$ to $\phi V2$, $\phi H1$ to $\phi H2$, $\phi V2$ to $\phi H1$, $\phi H2$ to Vog.
6. Avoid shorting output pins to ground or any low impedance source during operation.

CAUTION:

This device contains limited protection against Electrostatic Discharge (ESD). This device is rated as Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test.)

Devices should be handled in accordance with strict ESD protection procedures.



3.2 DC OPERATING CONDITIONS

Description	Symbol	Min	Nom	Max	Unit	Max DC Current (mA)	Notes
Reset Drain	Vrd	10.5	11	11.5	V	0.01	
Output Amplifier Return	Vss	1.5	2.0	2.5	V	0.45	
Output Amplifier Supply	Vdd	14.75	15	17	V	Iout	
Substrate	Vsub	0	0	0	V	0.01	
Output Gate	Vog	4.75	5.0	5.25	V	0.01	
Guard Ring	Vguard	9.5	10.0	10.5	V	0.01	
Video Output Current	Iout		-5	-10	mA	-	1

Notes:

1. An output load sink must be applied to Vout to activate output amplifier - see Figure below.

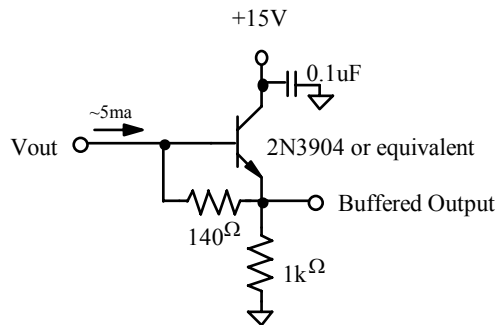


Figure 3 Typical Output Structure Load Diagram



3.3 AC OPERATING CONDITIONS

Description	Symbol	Level	Min.	Nom.	Max.	Units	Effective Capacitance	Notes
Vertical CCD Clock - Phase 1	$\phi V1$	Low	-9.5	-9.0	-8.5	V	24 nF (all $\phi V1$ pins)	1, 2
		High	0.5	2.0	1.5	V		
Vertical CCD Clock - Phase 2	$\phi V2$	Low	-9.5	-9.0	-8.5	V	24 nF (all $\phi V2$ pins)	1, 2
		High	0.5	2.0	1.5	V		
Horizontal CCD Clock - Phase 1	$\phi H1$	Low	-4.0	-4.0	-2.5	V	300 pF	1
		High	$\phi H1$ Low+1 0.0	$\phi H1$ Low+10. 0	$\phi H1$ Low+1 0.0	V		
Horizontal CCD Clock - Phase 2	$\phi H2$	Low	-4.0	-4.0	-2.5	V	200 pF	1
		High	$\phi H2$ Low+1 0.0	$\phi H2$ Low+10. 0	$\phi H2$ Low+1 0.0	V		
Reset Clock	ϕR	Low	4.0	5.0	6.0	V	10 pF	1
		High	9.0s	10.0	11.0	V		

Notes:

1. All pins draw less than 10uA DC current.
2. Capacitance values measured by examining the rise and fall times of the clock waveforms using clock drivers with known output impedance. This is the effective capacitance that the clock driver will see when operating the sensor.

3.4 AC TIMING CONDITIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes
$\phi H1, \phi H2$ Clock Frequency	f_H		4	12	MHz	1, 2, 3
Pixel Period (1 Count)	t_e	83	250		ns	
$\phi H1, \phi H2$ Setup Time	$t_{\phi HS}$	0.5	1		us	
$\phi V1, \phi V2$ Clock Pulse Width	$t_{\phi V}$	10	20		us	2
Reset Clock Pulse Width	$t_{\phi R}$	10	20		ns	4
Readout Time	$t_{readout}$	592	1719		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	287.8	836		us	7

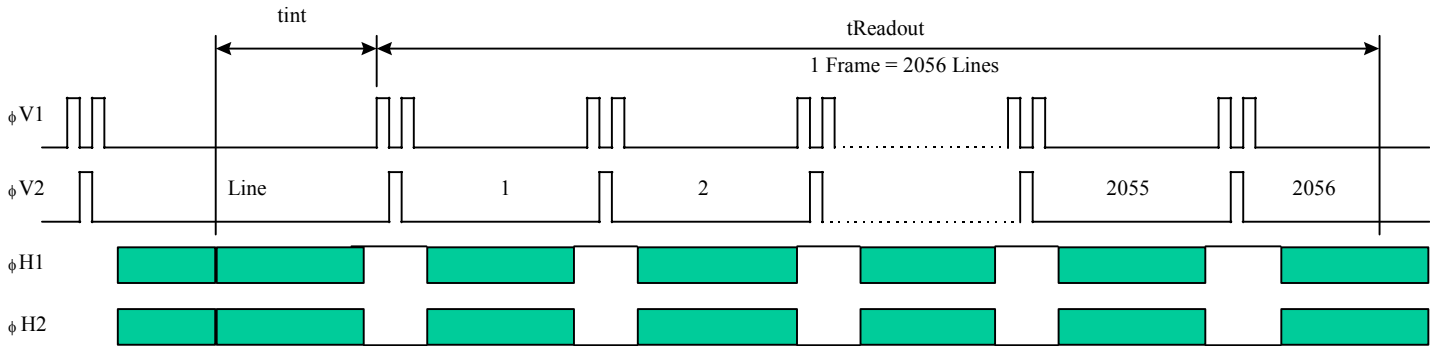
Notes:

1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Cross-over of register clocks should be between 40-60% of amplitude.
4. ϕR should be clocked continuously.
5. $t_{readout} = (2056 * t_{line})$
6. Integration time is user specified. Longer integration times will degrade noise performance.
7. $t_{line} = (3 * t_{\phi V}) + t_{\phi HS} + (3100 * t_e) + t_e$

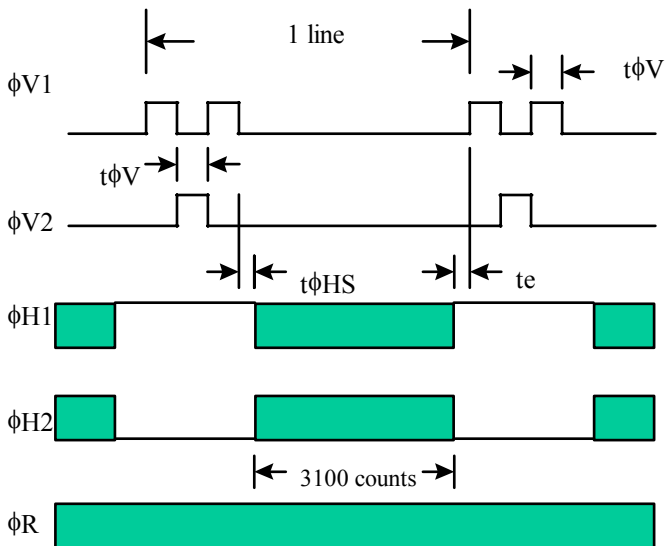


3.5 Clock Timing

Frame Timing



Line Timing Detail



Pixel Timing Detail

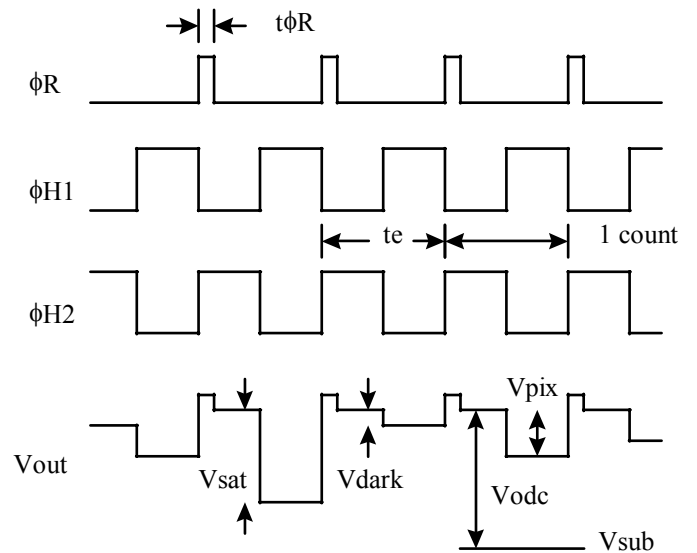


Figure 4 Timing Diagrams



4. ENVIRONMENTAL

4.1 Operating Conditions

	Environment	Minimum	Maximum	Units	Notes
Operating to Specification	Temperature	-25	+40	°C	1
	Humidity	5	90	%RH	1
Operating without Damage	Temperature	-25	+70	°C	2
	Humidity	5	90	%RH	2
In-Use Storage	Temperature	-20	+80	°C	
	Humidity	-	90	%RH	

Notes:

1. The image sensor shall meet the specifications of this document while operating at these conditions.
2. The image sensor shall continue to function but not necessarily meet the specifications of this document while operating at the specified conditions.

4.2 Reliability Testing

See Application Note MTD/PS-0292, Quality and Reliability, for the ISS environmental testing philosophy and procedures.

4.3 Inventory Storage

Image sensors should be stored at room temperature (nominally 25°C.) in dry nitrogen. This is particularly important for image sensors with temporary cover glass. Excessive humidity will degrade MTTF.

4.4 Electrostatic Discharge

CAUTION:

To allow for maximum performance, this device was designed with limited input protection; thus, it is sensitive to electrostatic induced damage. These devices should be installed in accordance with strict ESD handling procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test).

Devices should be stored in the conductive plastic, first-level packing.

For more information, see ISS Application Note MTD/PS-0224, Electrostatic Discharge Control.



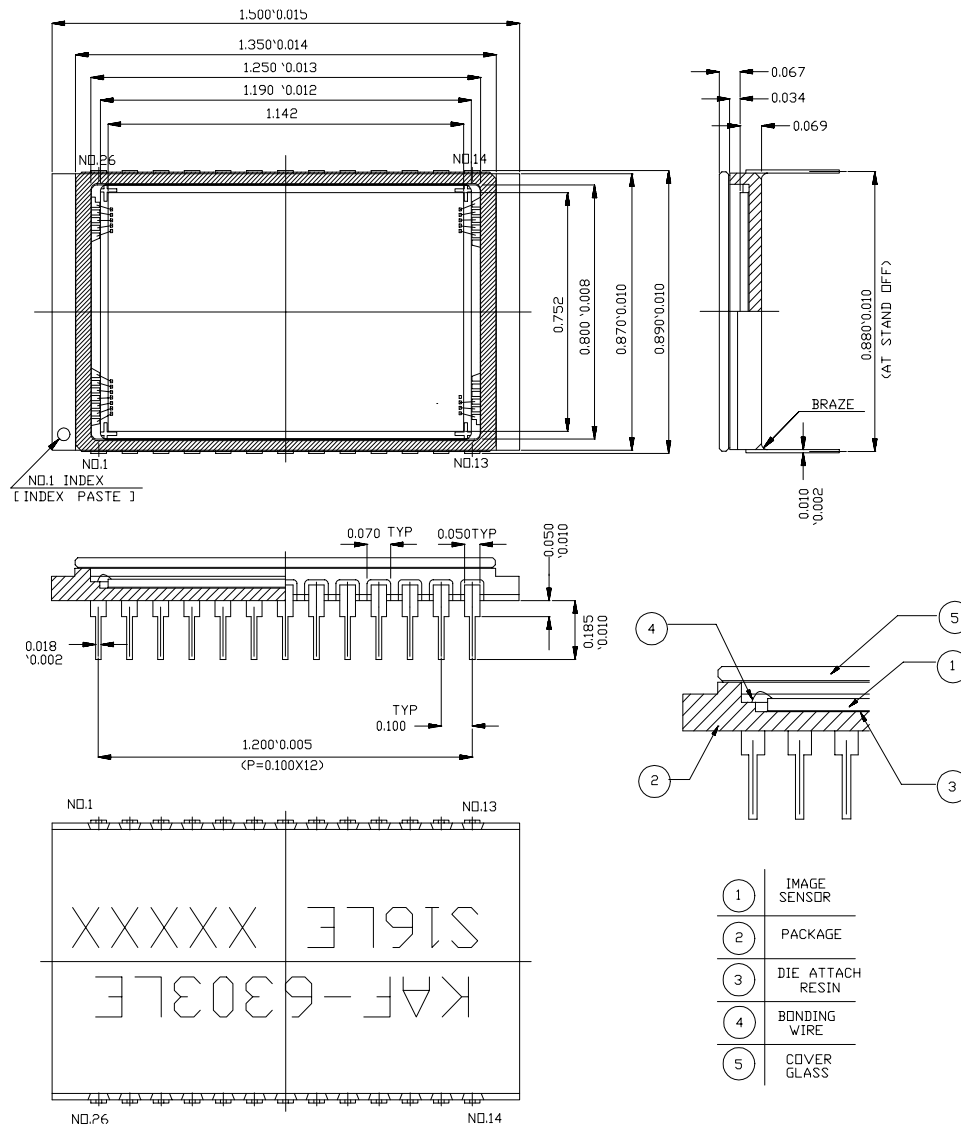
5. QUALITY ASSURANCE AND RELIABILITY

- 5.1 Quality Strategy:** All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.
- 5.2 Replacement:** All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.
- 5.3 Liability of the Supplier:** A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer
- 5.4 Liability of the Customer:** Damage from mechanical (scratches or breakage), electrical (ESD), or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.
- 5.5 Cleanliness:** Devices are shipped free of mobile contamination inside the package cavity. Immovable particles and scratches that are within the imager pixel area and the corresponding cover glass region directly above the pixel sites are also not allowed. The cover glass is highly susceptible to particles and other contamination. Touching the cover glass must be avoided. See ISS Application Note DS 00-009, Cover Glass Cleaning, for further information.
- 5.6 ESD Precautions:** Devices are shipped in static-safe containers and should only be handled at static-safe workstations. See ISS Application Note MTD/PS-0224 for handling recommendations.
- 5.7 Reliability:** Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. . For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.
- 5.8 Test Data Retention:** Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.
- 5.9 Mechanical:** The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.



6. MECHANICAL DRAWINGS

6.1 PACKAGE DRAWING



Eastman Kodak Company - Image Sensor Solutions
For the most current information regarding this product:

Phone: (585) 722-4385 Fax: (585) 477-4947 Web: www.kodak.com/go/imagers E-mail: imagers@kodak.com

7. Ordering Information

Address all inquiries and purchase orders to:

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Eastman Kodak Company
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Phone: (585) 722-4385
Fax: (585) 477-4947
Web: www.kodak.com/go/imagers
E-mail: imagers@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

Changes:

Revision Number	Release Date	Description of Changes
1	7/18/02	Initial formal release.

